IN THE CLAIMS

Please amend the claims as follows:

1. (Original) A method of determining time margins between strobe and data signals in an interface, comprising:

connecting an interface between two chips, at least one having a core and an input/output device;

providing data and strobe signals from said core to said interface;

providing a delay in one of said data and strobe signals within said interface;

varying said delay over a sequence of instructions; and

determining when errors occur and hence the maximum time margin available.

2. (Original) The method according to claim 1, further comprising:

providing a clock signal to said interface.

3. (Original) The method according to claim 2, further comprising:.

4. (Currently Amended) A method of determining time margins between strobe and data signals in an interface, comprising:

connecting an interface between two chips, at least one having a core and an input/output device;

providing data and strobe signals from said core to said interface;

providing a delay in one of said data and strobe signals within said interface;

varying said delay over a sequence of instructions;

providing a clock signal to said interface;

producing a data sync signal from said data signal and said clock signal;

producing a strobe sync signal from said strobe signal and said clock signal;

delaying said data signal and said data sync signal by the same amount;

delaying said strobe signal and said strobe sync signal by the same amount; and

determining when errors occur and hence the maximum time margin ~~available~~ available.

5. (Original) The method according to claim 4, wherein the data signal and data sync signal on the one hand and the strobe signal and strobe sync signal on the other hand are delayed in relation to each other so as to vary the setup and hold of the data with respect to the strobe.

6. (Currently Amended) A method of determining time margins between strobe and data signals in an interface, comprising:

connecting an interface between two chips, at least one having a core and an input/output device;

providing data and strobe signals from said core to said interface;

providing a delay in one of said data and strobe signals within said interface;

varying said delay over a sequence of instructions;

providing a clock signal to said interface;

producing a data sync signal from said data signal and said clock signal;

producing a strobe sync signal from said strobe signal and said clock signal;

determining when errors occur and hence the maximum time margin available; and.

~~The method according to claim 3~~, wherein said data sync signal is applied as a clock input to a first flipflop and said strobe sync signal is applied as a clock input to a second flipflop.

7. (Original) The method according to claim 6, wherein a data input of said first and second flipflops are connected to a transmit signal from the core.

8. (Original) An apparatus for determining a time margin in an interface, comprising:

two chips, at least one including a core and at least one input/output device;

an interface arranged between said two chips;

said interface receiving data and strobe signals from said core; and

a delay device provided within said interface for delaying one of said data and strobe signals, said delay device providing a variable delay so that the timing relationship between said data and said strobe signals can be varied until errors occur, thus providing the indication of the timing margin.

9. (Original) The apparatus according to claim 8, wherein said interface includes a data sync generator receiving said data signal and a clock signal to produce a data sync signal; and

a strobe sync signal generator receiving said strobe signal and said clock signal to produce a strobe sync signal.

10. (Currently Amended) An apparatus for determining a time margin in an interface, comprising:

two chips, at least one including a core and at least one input/output device;

an interface arranged between said two chips, said interface receiving data and strobe signals from said core, said interface including;

a data sync generator receiving said data signal and a clock signal to produce a data sync signal

a strobe sync signal generator receiving said strobe signal and said clock signal to produce a strobe sync signal and

a delay device provided within said interface for delaying one of said data and strobe signals, said delay device providing a variable delay so that the timing relationship between said data and said strobe signals can be varied until errors occur, thus providing the indication of the timing margin;[[0]]

a first flipflop, said first flipflop receiving said data sync signal as a clock input and

a second flipflop receiving said strobe sink signal as a clock input.

11. (Original) The apparatus according to claim 10, wherein said delay device includes four delay elements receiving said data signal, said data sync signal, said strobe signal and said strobe sync signal.

12. (Original) The apparatus according to claim 11, wherein said delay elements for receiving said data signal and data sync signal have the same delay and the delay elements receiving the strobe signal and strobe sync signal have the same delay.

13. (Original) A method for determining timing margining in a high speed source synchronous interface comprising:

providing a data signal;

providing a strobe signal;

changing the relationship in time between said strobe signal and said data signal so as to vary the setup and hold of data with respect to strobe;

detecting when a failure occurs so as to determine the maximum time margin.

14. (Original) The method according to claim 13, wherein said high speed source synchronous interface is arranged between two chips of a chip set.

15. (Previously Presented) The method according to claim 13, wherein the changing relationship between said strobe signal and said data signal in time includes changing a delay of one of the strobe and data signals.